IJAREEIE

e-ISSN: 2278-8875
p-ISSN: 2320-3765

International Journal of Advanced Research

in Electrical, Electronics and Instrumentation Engineering

Volume 10, Issue 1, January 2021

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 7.122

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|| A Monthly Peer Reviewed & Refereed Journal |

||Volume 10, Issue 1, January 2021||

|DOI:10.15662/IJAREEIE.2021.1001029|

Enhancing Ubiquitous Healthcare with Hardware-Accelerated WBSNs

Sahana Devadiga[1*], Ashwini Kundanagar[2*]

Lecturer, Department of E&E, Government Polytechnic Udupi, Karnataka, India[1*]

Lecturer, Department of E&C, Government Polytechnic Udupi, Karnataka, India[2*]

ABSTRACT: The Wireless Body Sensor Network (WBSN) is gaining significant attention due to its relevance to human living environments. With the rise in chronic diseases attributed to unhealthy lifestyles, the role of WBSNs has become increasingly important. Initially developed for military use—where soldiers could monitor their own health conditions—WBSNs proved valuable in detecting health anomalies during combat, enabling timely preventive actions. This success spurred extensive research and growth in biomedical applications. This paper focuses on the development of a hardware accelerator specifically for WBSNs. The accelerator is designed to process four key health parameters: Blood Pressure (BP), Electrocardiogram (ECG), Body Temperature, and Electroencephalogram (EEG). The design is implemented, simulated, and synthesized using an FPGA from the Virtex-7 family. The proposed system offers advantages in terms of lower power consumption and enhanced processing speed.

KEYWORDS: WBSN, FPGA

I. INTRODUCTION

Wireless Body Sensor Networks (WBSNs) are currently receiving significant attention in the realm of biomedical applications. With the global population on the rise, there is a growing need to develop user-friendly devices capable of monitoring health parameters conveniently. This demand has led to extensive research in the biomedical field.Elderly individuals often face poor health conditions, which can be worsened by inadequate living environments. Such circumstances are increasingly affecting younger populations as well. Therefore, there is a pressing need for systems that allow individuals to monitor their health without the constant need for medical consultations.Chronic illnesses such as cancer and cardiovascular diseases are impacting large segments of the population. Early detection of these conditions is essential, as it allows for timely treatment and can potentially save lives. As part of this effort, considerable work is being done in the development of WBSNs.Effective WBSN devices should be capable of processing multiple bio-signals. These signals are captured using sensors that may be externally worn or implanted inside the body. The output from these sensors must be processed efficiently and transmitted wirelessly via Bluetooth, Wi-Fi, or Zigbee. Real-time operation is crucial to ensure accurate and timely diagnostics.Recent studies have introduced hardware-focused architectures for WBSNs that are designed to consume minimal power and support long-term usage. Techniques such as adaptive power control and fuzzy control systems are commonly used for processing bio-signals. Health parameters like blood pressure (BP), body temperature, ECG, and EEG are handled using a Multi-Controller Unit (MCU).

The proposed architecture includes four main modules: a register array, a predictor, an encoder, and an error control coding (ECC) unit. Initially, the sensor data is stored temporarily in the register array. From the array of four sensor values, a predictor estimates one representative value based on historical data, which significantly reduces processing time compared to handling all values individually.Next, the predicted values are compressed using an appropriate compression algorithm to minimize data size, thus reducing transmission time. Signal compression must be efficient to meet required bitrates while keeping the system complexity low. To secure patient information during wireless transmission, the data is encrypted using robust algorithms. Since wireless communication is vulnerable to external threats, encryption is critical for safeguarding personal health information.After encryption, the data undergoes error control coding to enhance reliability and ensure error-free transmission. This combination of techniques ensures that bio-signals are securely and accurately transmitted. With these components, a dedicated hardware accelerator can be built to support the efficient, real-time, and secure transmission of multiple health signals.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|| A Monthly Peer Reviewed & Refereed Journal |

||Volume 10, Issue 1, January 2021||

|DOI:10.15662/IJAREEIE.2021.1001029|

II. WIRELESS BODY SENSOR NETWORK SYSTEM

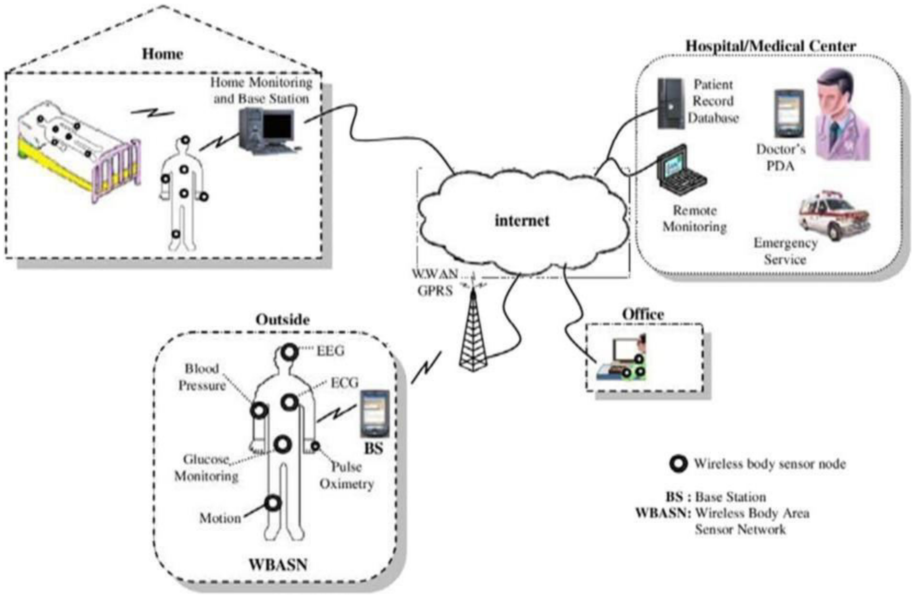

Fig.2.1 Wirelessbodysensornetworksystem

Figure 2.1 illustrates a typical Wireless Body Sensor Network (WBSN) system, depicting patients in various environments such as at home, in the office, and outdoors. The system is designed to be compatible across all these scenarios. Sensors are either embedded in or attached to the patient's body to continuously monitor health parameters.These sensors collect vital data—such as blood pressure, body temperature, electroencephalogram (EEG), electrocardiogram (ECG), glucose levels, pulse oximetry, and motion activity. The gathered information is processed locally and transmitted wirelessly to a medical center or hospital, ensuring that healthcare professionals can receive timely updates for evaluation and intervention.

Each patient's body comprises multiple sensor nodes that collect data and transmit it to a central node, typically located on the body or nearby. Due to the wireless nature of the communication, the central node plays a critical role in data processing. Wireless transmissions are prone to data loss or corruption; hence, reliable processing and secure transmission of data from the central node to healthcare providers is essential. At the receiving end, medical personnel can decrypt the information using appropriate algorithms, analyze the data, and provide timely support such as telemedicine consultations or emergency medical services. The sensor nodes are generally compatible with 2.4 GHz communication bands, allowing seamless data transmission.

Classification of Sensors in WBSNs

Sensors used in Body Sensor Networks (BSNs) are broadly classified based on the type of physiological signals they measure:

1. **Continuous Signal Sensors:**These include accelerometers, gyroscopes, ECG, EEG, and EMG sensors. They are designed to continuously monitor physiological activity, producing large volumes of real-time data. Due to their constant operation, these sensors typically result in high data transmission rates and increased energy consumption.
2. **Periodic Signal Sensors:**This group comprises glucose monitors, temperature sensors, moisture sensors, blood pressure sensors, and blood oxygen saturation sensors. These devices collect specific physiological data at regular intervals rather than continuously, resulting in lower energy consumption and less frequent data transmissions.

Applications of Wireless Sensor Networks (WSNs)

1. Telemedicine and Remote Patient Monitoring:Telemedicine leverages advanced health information systems and telecommunications technologies to deliver medical care remotely. This approach enables healthcare professionals, including doctors and researchers, to reach patients regardless of location. Remote patient monitoring, particularly in

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|| A Monthly Peer Reviewed & Refereed Journal |

||Volume 10, Issue 1, January 2021||

|DOI:10.15662/IJAREEIE.2021.1001029|

home settings, allows for the consistent tracking of patients' health, especially for those with chronic conditions. This technology can significantly enhance patient outcomes and quality of life.

2. Biofeedback Systems:Biofeedback involves monitoring and analyzing physiological parameters to help users learn how to control certain bodily functions consciously. Devices placed on the surface of the body provide feedback, enabling users to adjust their physical activity, reduce stress, or manage health conditions more effectively. This technique supports performance improvement and wellness through self-regulation guided by real-time physiological data.

III. MODELING AND ANALYSIS

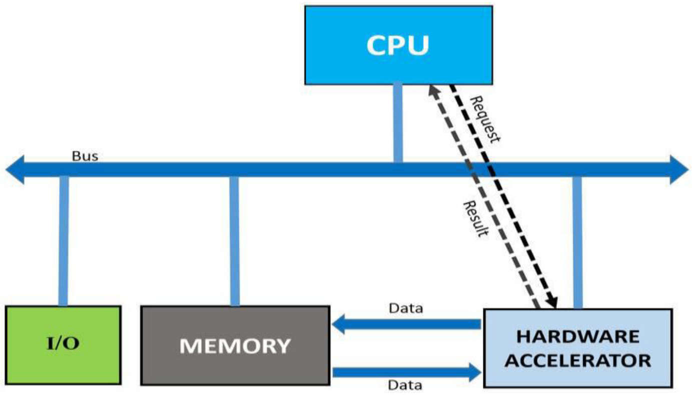

Fig:3.1 Basic Hardware Accelerator architecture

Hardware Accelerator Architecture for WBSN

In this architecture (illustrated in Fig. 3.1), the CPU offloads specific tasks to the FPGA, which executes them and returns the results efficiently. The section below outlines the characteristics of various evaluated hardware accelerators. Vision kernels have been categorized based on their functional features to better understand how these features impact kernel performance on different hardware architectures.

1. Central Processing Unit (CPU):

Modern CPUs support SIMD (Single Instruction, Multiple Data) instructions through multiple Arithmetic Logic Units (ALUs). These SIMD instructions are particularly useful for image processing, where the same operation is repeated across a large stream of data—common in computer vision applications. Examples of SIMD architectures include ARM NEON and Intel's SSE (Streaming SIMD Extensions).

2. Graphics Processing Unit (GPU):

GPUs are specialized for SIMD operations and are optimized for parallel image processing. Unlike general-purpose CPUs, GPUs consist of a large number of simpler processing cores with minimal control logic, no complex branch prediction, and limited per-core memory. This design enables GPUs to host more cores per chip. They perform best in workloads with low branching and high data parallelism. Additionally, GPUs have high-throughput memory systems tailored for fast image data streaming. For instance, the Jetson TX2 (Pascal GPU) includes a 2048 KB L2 cache for high-speed processing of 1080p grayscale images.

3. Field Programmable Gate Array (FPGA):

FPGAs do not use a traditional processor-based architecture. Instead, they consist of configurable logic blocks, DSPs, on-chip BRAMs (Block RAMs), I/O pads, and routing channels. These components allow designers to create custom data paths to stream pixel data between memory and processing units efficiently. FPGAs also enable localized memory access via distributed BRAMs. For example, the Zynq UltraScale MPSoC FPGA offers 32.1 MB of on-chip memory, optimizing data locality for vision kernels. However, developers must ensure that their custom FPGA designs meet both timing and area constraints.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|| A Monthly Peer Reviewed & Refereed Journal |

||Volume 10, Issue 1, January 2021||

|DOI:10.15662/IJAREEIE.2021.1001029|

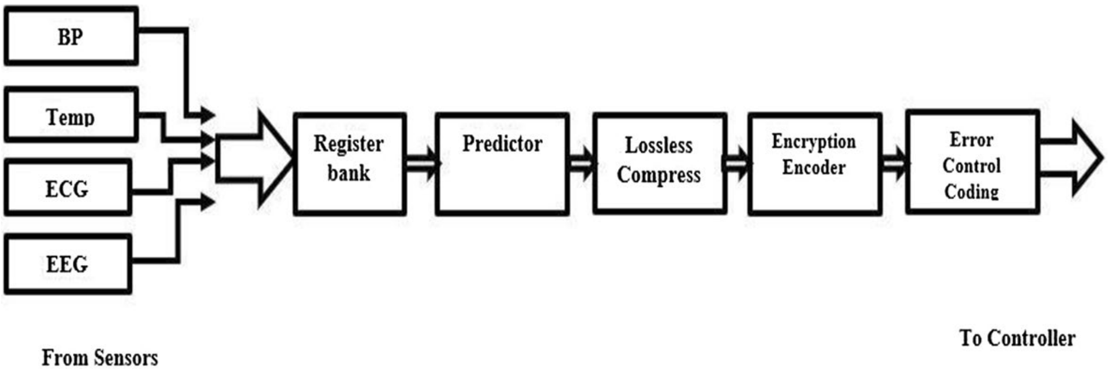

Fig.3.2 Architecture of hardware accelerator for WSN

Proposed Hardware Accelerator for WBSN

The proposed hardware accelerator (illustrated in Fig. 3.2) is designed to be cost-effective and energy-efficient for Wireless Body Sensor Networks (WBSN).
Signal Detection & Conversion:Bio-signals such as blood pressure, temperature, EEG, and ECG are captured by sensors placed on or inside the body. These analog signals are converted to digital using an ADC (Analog-to-Digital Converter).
Register Bank Storage:The digitized signals are stored in a register bank or register array, where each parameter has four recorded values (latest and previous three).
Prediction Stage:A predictor module, based on mathematical models and a trending tree algorithm, processes these four values to predict the next value for each parameter.

Compression and Encryption:
The predicted values are compressed using a lossless technique and then encrypted for security. To ensure reliable transmission, Error Control Coding (ECC) is applied.

Transmission:After processing, the encrypted and encoded data is sent to a controller for wireless transmission.At the hospital end (shown in Fig. 4.2), the transmitted data is received via antenna and goes through decryption, ECC decoding, and decompression. Medical professionals analyze the data to monitor the patient. Any abnormalities trigger alerts for the patient or caregivers.

Register Array Circuit Details
To manage four different bio-signals, a register array circuit was implemented as shown in Fig. 3.3. Each register bank handles one signal and includes four D flip-flops, connected to form shift registers. The ADC output, which is 12 bits wide, is stored in these registers. As new values arrive, previous values are shifted to the right:The most recent value is stored in the first flip-flop.Upon arrival of the next value, is shifted to the next flip-flop, and so on.This mechanism stores the current and last three values: .These stored values are then passed to the predictor and compressor, forming the critical input for further data processing.

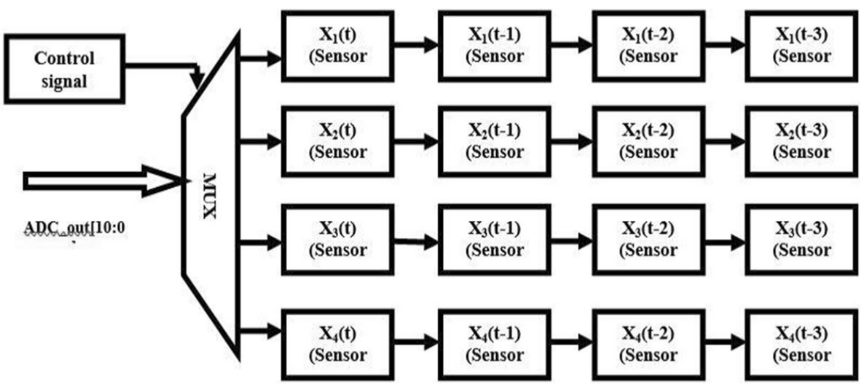

Fig. 3.3 Register array

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|| A Monthly Peer Reviewed & Refereed Journal |

||Volume 10, Issue 1, January 2021||

|DOI:10.15662/IJAREEIE.2021.1001029|

Predictor Block

The predictor module estimates the next value of each physiological parameter using the four most recent readings stored in the register array. In the context of Wireless Body Sensor Networks (WBSN) [5], prediction plays a vital role in minimizing processing time, which is essential due to the system's strict timing requirements. Each body parameter is represented in the register bank by four consecutive values and .These values are fed into the predictor circuit, as illustrated in Figure 4.4.The predictor performs three key functions to compute the next predicted value. Initially, the differences between the four values are calculated using Equations 1 and 2. Then, using Equations 3, 4, and 5, the predictor applies three mathematical functions to derive an accurate estimate of the upcoming data point.

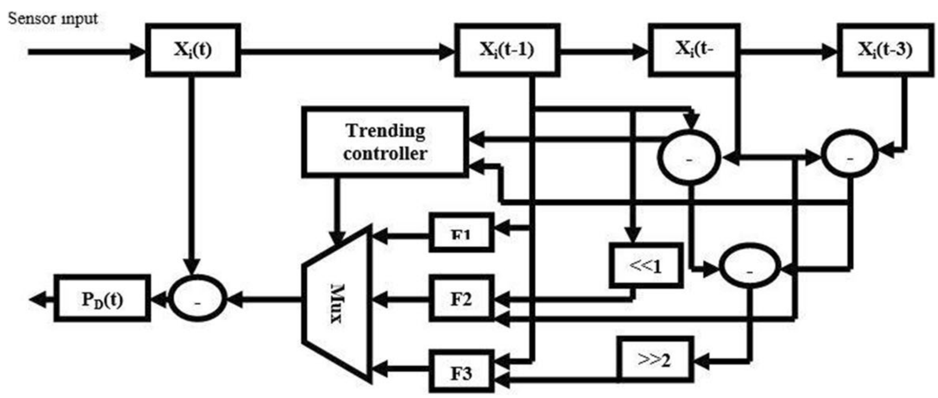

Fig. 3.4 Predictor

$$Diff1 = Xi[t-1] - Xi[t-2]$$

$$Diff2 = Xi[t-2] - Xi[t-3]$$

Adaptive Fuzzy Prediction

To enhance the effectiveness of lossless encoding algorithms, both first-order and second-order prediction techniques have been used. These are based on linear and slope-based prediction methods, respectively [1,6]. While second-order prediction is generally more accurate—particularly in regions of the ECG signal that exhibit rapid changes (steep slopes)—first-order prediction proves to be more reliable in smoother segments of the signal.

To balance the strengths of both methods, an adaptive fuzzy decision control approach is introduced. This technique dynamically selects the most appropriate prediction method based on the characteristics of the signal, as illustrated in Figure 4.5.The adaptive fuzzy prediction process consists of four main steps:

1. Input Calculation:The current signal value is predicted using the three previous values: , , and . A fuzzy decision mechanism drives this prediction process.
2. Difference Evaluation:Two differences are computed:Their absolute values are then compared to a threshold to determine whether the differences are high or low.
3. Slope Direction Classification:The signs (slopes) of Diff1 and Diff2 are compared to assess whether they are changing in the same direction or in opposite directions.
4. Prediction Function Selection:

Based on the difference magnitudes and slope directions, the fuzzy controller selects one of four prediction functions (F1, F2, F3, F4). Each function is tailored to perform better under specific signal conditions.

By adapting the prediction method in real time, this fuzzy logic-based approach significantly improves prediction accuracy, thereby optimizing compression efficiency in ECG signal processing.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|| A Monthly Peer Reviewed & Refereed Journal |

||Volume 10, Issue 1, January 2021||

|DOI:10.15662/IJAREEIE.2021.1001029|

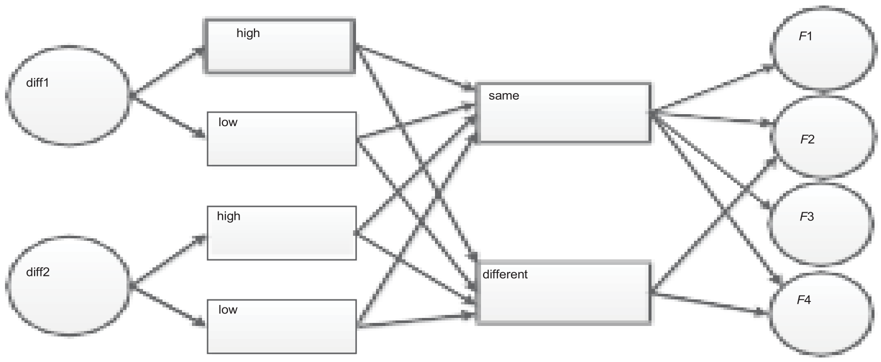

Fig.3.5 Adaptive fuzzy prediction equations

diff1= x(n–2)-x(n–3)

diff2= x(n–1)-x(n–2)

F 1: x'(n)=x(n–1)

F 2: x'(n)=2x(n–1)+x(n–2)

F 3: x'(n)=(x(n–1)+x(n–2))/2

F 4: x'(n)=x(n–1)+(x(n–1)–x(n–2))/2

Encryption

After predicting a single body parameter value from the set of four, it becomes essential to secure the data using an encryption algorithm, ensuring the confidentiality of patient information. Protecting this sensitive data from unauthorized access is a key requirement in medical systems.

The encryption method employed here uses multiplexers (MUXes). Each MUX uses select lines as encryption keys. The predicted 12-bit data is fed into a series of multiplexers, as shown in Figure 4.6. The select lines determine which bit from the predicted data is output, effectively scrambling the information to produce the encrypted output.The number of multiplexers corresponds to the 12-bit size of the data (since ADC output is 12 bits).Because the bits can be rearranged in 12! (47,90,01,600) ways, the encryption key space is very large, making it extremely difficult for an attacker to guess or crack the encryption.At the receiving end, the decryption process reverses the MUX-based scrambling to recover the original predicted data using the same key (select lines).

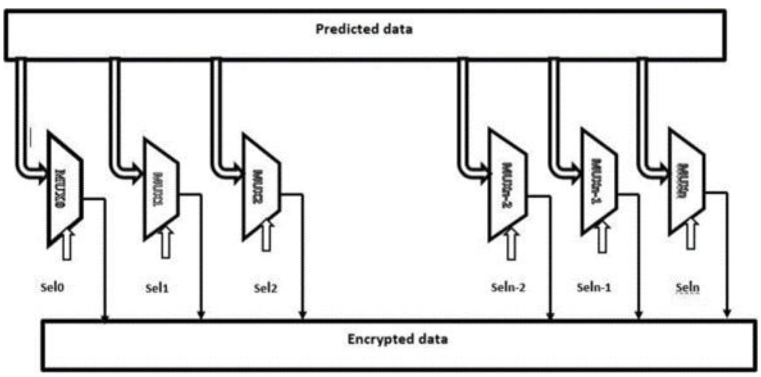

Fig. 3.6 Encryption

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|| A Monthly Peer Reviewed & Refereed Journal |

||Volume 10, Issue 1, January 2021||

|DOI:10.15662/IJAREEIE.2021.1001029|

Error Control Coding (ECC)

To ensure reliable data transmission, Error Control Coding is applied immediately after encryption. This technique involves:

1. Adding a parity bit to detect errors.
2. Inserting redundancy bits, which are extra bits created by flipping selected bits (0 to 1 or 1 to 0) in a known pattern.These additional bits allow the system to detect and correct errors during wireless transmission.At the receiver end, the redundancy bits are extracted and compared with newly calculated parity and flip indicators.If the values match, the data is considered correct.If mismatches occur, the system can identify and potentially correct the error.By using this method, ECC greatly reduces the chance of transmission errors and enhances the reliability of bio-signal communication. Simulations have shown that counting the number of flipped bits helps assess the accuracy of received data effectively.

IV. RESULTS AND DISCUSSION

Field-Programmable Gate Array (FPGA)

A Field-Programmable Gate Array (FPGA) is a type of integrated circuit that can be programmed by designers or users after manufacturing, hence the name field-programmable. Its configuration is typically defined using a Hardware Description Language (HDL), similar to the approach used for Application-Specific Integrated Circuits (ASICs).

Architecture and Functionality

FPGAs consist of an array of programmable logic blocks and hierarchical interconnects that allow these blocks to be flexibly connected. These logic blocks can be programmed to perform basic operations like AND and XOR, or more complex combinational logic. They also often include memory elements, ranging from simple flip-flops to entire memory blocks.

A key advantage of FPGAs is their reconfigurability, enabling them to be reprogrammed multiple times to support various logic functions. This makes FPGAs ideal for reconfigurable computing, a concept similar to how software operates on general-purpose processors.

Use in Embedded Systems

FPGAs play a crucial role in embedded system development by allowing:

- Concurrent hardware and software development
- Early system simulation and performance analysis
- Multiple design trials and architectural explorations before final implementation

Design Process

To program an FPGA, developers typically write their design in HDL (VHDL or Verilog) or use a schematic editor:HDLs are preferred for larger, more abstract designs Schematic entry is better for visualizing simpler or modular systems.Using Electronic Design Automation (EDA) tools, the HDL design is converted into a technology-mapped netlist. This netlist is then implemented onto the FPGA through a place-and-route process, usually using vendor-specific software.The design is verified through:Timing analysis,Simulation,Other validation techniques.Once verified, a binary configuration file is generated and loaded onto the FPGA via JTAG or external memory (e.g., EEPROM).

Languages and Tools:Verilog is widely used due to its C-like syntax, abstracting implementation details and simplifying design. SystemVerilog and VHDL are also popular for different applications and levels of abstraction.IP Cores and Libraries:To ease the design of complex systems, Intellectual Property (IP) cores—pre-tested and optimized functional blocks—are used. These are available from FPGA manufacturers or third-party vendors, enabling faster and more reliable development.

Simulation Stages

FPGA developers simulate the design at various stages:

1. RTL Simulation: Using test benches to verify the high-level HDL code.
2. Post-Synthesis Simulation: After HDL is converted to a gate-level netlist.
3. Timing Simulation: After final layout, with propagation delays back-annotated to check real-world timing behavior.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|| A Monthly Peer Reviewed & Refereed Journal |

||Volume 10, Issue 1, January 2021||

|DOI:10.15662/IJAREEIE.2021.1001029|

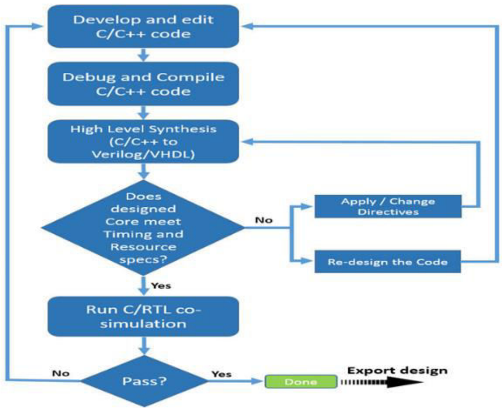

Fig 4.1 General design flow in Vivado HLS

Universal Asynchronous Receiver Transmitter (UART) Interface

To transmit the bitstream generated after applying Error Control Coding (ECC), a standard communication protocol like UART is employed. UART facilitates serial communication between the hardware (such as an FPGA-based accelerator) and external devices like a personal computer (PC). This interface plays a key role in hardware verification of the proposed accelerator by allowing seamless data exchange with external systems. By incorporating encryption and ECC before transmission, UART communication helps effectively address issues like bit errors, data loss, and security vulnerabilities during wireless data transmission.

V. CONCLUSION

Body Sensor Networks (BSNs) are composed of compact and intelligent sensors that are either implanted inside the body or attached to its surface to monitor and transmit both routine and emergency physiological data. These networks must be capable of promptly and reliably alerting healthcare providers in the event of physiological abnormalities.Designing a sensor network that fulfills the diverse and demanding requirements of healthcare applications is a complex task. To address these challenges, a cost-effective and energy-efficient hardware accelerator was developed and implemented on an FPGA platform specifically for Wireless Body Sensor Networks (WBSNs).

A novel register array was introduced to process four signal samples of each physiological parameter. Along with this, a predictor and a flexible encryption algorithm were designed to reduce transmission power and minimize diagnostic errors. The integration of encryption ensures confidentiality of personal health data during wireless communication.Furthermore, Error Control Coding (ECC) techniques were applied to enhance data reliability, allowing for more accurate readings of vital signs such as heart rate. The entire system was functionally verified using Vivado v2020.1, confirming its ability to process and wirelessly transmit data through a high-performance, low-power microcontroller. This accelerator design proves to be a highly suitable solution for developing next-generation WBSN systems.

REFERENCES

1.Mavinkattimath, Swati G., Rajashri Khanai, and Dattaprasad A. Torse. "FPGA implementation of a Micro controller Unit for Body Sensor Network." In 2018 International Conference on Computational Techniques, Electronics and Mechanical Systems (CTEMS), pp. 75-79. IEEE, 2018.
2.Mavinkattimath, Swati G., Rajashri Khanai, and Dattaprasad A. Torse. "A survey on secured wireless body sensor networks." In 2019 International Conference on Communication and Signal Processing (ICCSP), pp. 0872-0875. IEEE, 2019.
3.Sun, Xiao, Zongqing Lu, Xiaomei Zhang, Marcel Salathé, and Guohong Cao. "Infectious disease containment based on a wireless sensor system." Ieee Access 4 (2016): 1558-1569.
4.Chen, Chiung-An, Shih-Lun Chen, Hong-Yi Huang, and Ching-Hsing Luo. "An asynchronous multi-sensor micro control unit for wireless body sensor networks (WBSNs)." Sensors 11, no. 7 (2011): 7022-7036.
5.Chen, Shih-Lun, Min-Chun Tuan, Ho-Yin Lee, and Ting-Lan Lin. "VLSI implementation of a cost-efficient micro control unit with an asymmetric encryption for wireless body sensor networks." Ieee Access 5 (2017): 4077-4086.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|| A Monthly Peer Reviewed & Refereed Journal |

||Volume 10, Issue 1, January 2021||

|DOI:10.15662/IJAREEIE.2021.1001029|

6.Chen, S-L., G-A. Luo, and T-L. Lin. "Efficient fuzzy-controlled and hybrid entropy coding strategy lossless ECG encoder VLSI design for wireless body sensor networks." Electronics Letters 49, no. 17 (2013): 1058-1060.

7.Chen, S-L., and J-G. Wang. "VLSI implementation of low-power cost-efficient lossless ECG encoder design for wireless healthcare monitoring application." Electronics Letters 49, no. 2 (2013): 91-93.